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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
IQBAL, NADEEM	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,121	ADL-TABATABAI ET AL.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21 and 23-27* is/are rejected.

7)☒ Claim(s) *20 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1 & 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hohensee et al., (U.S. Patent number 5778211).

4. As per claim 1, Hohensee et al., teaches (col. 3, lines 11-13) a control system that provides a series of instructions to the precise exception handling processor to facilitate emulation of at least one instruction from an emulated program. He thus teaches an instruction bundle that comprises a first instruction, a second instruction, and the second instruction that includes a pointer to an exception handler. He does not explicitly disclose that the second instruction includes a predetermined offset from the first instruction. He teaches (col. 3, lines 17-19) that if an exception is detected during processing of an instruction, the exception condition is

processed in connection with a subsequent instruction. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to realize that He would also include a second instruction with a predetermined offset from the first instruction. This is because that with the detection of an exception condition during processing, the exception condition is processed in connection with a subsequent instruction, thereby providing an offset from the first instruction.

5. As per claim 2, He teaches as stated above that if an exception is detected during processing of an instruction, the exception condition is processed in connection with a subsequent instruction, therefore the offset would include a predetermined number of instructions between the first instruction and the second instruction.

6. Claims 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hohensee et al., (U.S. Patent number 5778211) as applied to claims 1 & 2 above, and further in view of Corrie et al., (U.S. Patent number 6496926).

7. As per claims 3 & 4, Hohensee does not explicitly disclose that the second instruction includes a plurality of non-executable bits. Corrie teaches (col. 7, lines 36-38) a computer implemented exception handler. He further teaches a "NOP" instruction that does not change the state of the code space, and also teaches that the NOP instructions are used to link threads of code together in the code space. It would have been obvious to a person of ordinary skill in the art to realize that Hohensee would also include the NOP instructions, since Hohensee teaches a series of instructions to the precise exception handler that would require instructions to link threads of code, therefore would include NOP instructions which include non-executable bits.

8. As per claims 5 & 6, Corrie teaches a "NOP" instruction that does not change the state of the code space, and also teaches that the NOP instructions are used to link threads of code together in the code space, therefore would precedes the first instruction.

9. As per claim 7, Hohensee teaches (col. 3, lines 17-19) that if an exception is detected during processing of an instruction, the exception condition is processed in connection with a subsequent instruction.

10. As per claim 8, Hohensee teaches (col. 8, lines 7-10) a microprocessor 11 used in emulation of a microprocessor which features a delayed exception handling model, and that Intel x86 family also features delayed exception handling, therefore making his invention bundle compatible with IA64 instruction bundle.

11. As per claim 9, Corrie teaches a "NOP" instruction that does not change the state of the code space, these instructions would include unused bit space.

12. Claims 10 & 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hohensee et al., (U.S. Patent number 5778211) in view of Corrie et al., (U.S. Patent number 6496926).

13. As per claim 10, Hohensee et al., substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches (col. 3, lines 11-13) a control system that provides a series of instructions to the precise exception handling processor to facilitate emulation of at least one instruction from an emulated program. He thus teaches an instruction bundle that comprises a first instruction, a second instruction, and the second instruction that includes a pointer to an exception handler. Hohensee does not explicitly disclose that the second instruction includes a NOP instruction that includes a pointer to an exception handler. Corrie teaches (col. 7, lines 36-38) a computer implemented exception handler. He further teaches a "NOP" instruction that does

not change the state of the code space, and also teaches that the NOP instructions are used to link threads of code together in the code space. It would have been obvious to a person of ordinary skill in the art to realize that Hohensee would also include the NOP instructions, since Hohensee teaches a series of instructions to the precise exception handler that would require instructions to link threads of code, therefore would include NOP instructions which include non-executable bits.

14. As per claim 11, Hohensee teaches (col. 8, lines 7-10) a microprocessor 11 used in emulation of a microprocessor which features a delayed exception handling model, and that Intel x86 family also features delayed exception handling, therefore making his invention bundle compatible with IA64 instruction bundle.

15. Claims 12-19, 21, 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hohensee et al., (U.S. Patent number 5778211).

16. As per claim 12, Hohensee et al., teaches (col. 3, lines 11-13) a control system that provides a series of instructions to the precise exception handling processor to facilitate emulation of at least one instruction from an emulated program. He thus teaches a method of handling an exception comprising executing a first instruction. He also teaches (col. 3, lines 17-19) that if an exception is detected during processing of an instruction, the exception condition is processed in connection with a subsequent instruction. He thus teaches limitations pertain to the first instruction returns an exception. He does not explicitly disclose using a program counter to determine the location of a second instruction, wherein the second instruction includes a pointer to an exception handler. He teaches (col. 3, lines 32-34) that if an exception condition is detected during the processing operations, to invoke an exception handler in accordance with the

processor's precise exception handling model. It would have been obvious to a person of ordinary skill in the art to realize that His control system would also include a program counter to determine the location of a second instruction that includes a pointer to an exception handler. This is because, his control system provides a series of instruction, detection of exception handling conditions and mechanism to invoke an exception handler. Furthermore, it is well know in the art to utilize a program counter to determine the location of the next instruction to be executed.

17. As per claim 13, He teaches as stated above that if an exception is detected during processing of an instruction, the exception condition is processed in connection with a subsequent instruction, therefore the pointer would include a number of instructions between a subsequent instruction and the exception handler.

18. As per claim 14, He teaches (col. 3, lines 32-34) that if an exception condition is detected during the processing operations, to invoke an exception handler in accordance with the processor's precise exception handling model.

19. As per claims 15 & 16, He teaches as stated above that if an exception is detected during processing of an instruction, the exception condition is processed in connection with a subsequent instruction, therefore the pointer would include a number of instructions between a subsequent instruction and the exception handler.

20. As per claims 17 & 18, He teaches as stated above that if an exception is detected during processing of an instruction, the exception condition is processed in connection with a subsequent instruction, therefore the offset would include a predetermined number of instructions between the first instruction and the second instruction.

21. As per claim 19, He teaches (col. 4, lines 29-31) to invoke an exception handler in accordance with the precise exception handling processor's precise exception handling model. He thus would also include a plurality of types of exception handlers.

22. As per claim 21, Hohensee et al., teaches (col. 3, lines 11-13) a control system that provides a series of instructions to the precise exception handling processor to facilitate emulation of at least one instruction from an emulated program. He thus would include an instruction bundle.

23. As per claim 23, Hohensee et al., substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches (col. 3, lines 11-13) a control system that provides a series of instructions to the precise exception handling processor to facilitate emulation of at least one instruction from an emulated program. He thus teaches a compiled code segment that comprises a first instruction, a second instruction, and the second instruction that includes a pointer to an exception handler. Hohensee does not explicitly disclose a NOP instruction that includes a pointer to an exception handler. Corrie teaches (col. 7, lines 36-38) a computer implemented exception handler. He further teaches a "NOP" instruction that does not change the state of the code space, and also teaches that the NOP instructions are used to link threads of code together in the code space. It would have been obvious to a person of ordinary skill in the art to realize that Hohensee would also include the NOP instructions, since Hohensee teaches a series of instructions to the precise exception handler that would require instructions to link threads of code, therefore would include NOP instructions which include non-executable bits.

24. As per claims 24 & 25, Hohensee et al., teaches (col. 3, lines 11-13) a control system that provides a series of instructions to the precise exception handling processor to facilitate

emulation of at least one instruction from an emulated program. He thus teaches a method of handling an exception comprising executing a first instruction. He also teaches (col. 3, lines 17-19) that if an exception is detected during processing of an instruction, the exception condition is processed in connection with a subsequent instruction. He thus teaches limitations pertain to the first instruction returns an exception. He does not explicitly disclose using a program counter that indirectly points to an exception handler. He teaches (col. 3, lines 32-34) that if an exception condition is detected during the processing operations, to invoke an exception handler in accordance with the processor's precise exception handling model. It would have been obvious to a person of ordinary skill in the art to realize that His control system would also include a program counter to determine the location of a second instruction that includes a pointer to an exception handler. This is because, his control system provides a series of instruction, detection of exception handling conditions and mechanism to invoke an exception handler. Furthermore, it is well know in the art to utilize a program counter to determine the location of the next instruction to be executed.

25. As per claim 26, Hohensee et al., teaches (col. 3, lines 11-13) a control system that provides a series of instructions to the precise exception handling processor to facilitate emulation of at least one instruction from an emulated program. He thus teaches a method of handling an exception comprising executing a first instruction. He also teaches (col. 3, lines 17-19) that if an exception is detected during processing of an instruction, the exception condition is processed in connection with a subsequent instruction. He thus teaches limitations pertain to the first instruction returns an exception. He does not explicitly disclose using a program counter to determine the location of a second instruction, wherein the second instruction includes a pointer

to an exception handler. He teaches (col. 3, lines 32-34) that if an exception condition is detected during the processing operations, to invoke an exception handler in accordance with the processor's precise exception handling model. It would have been obvious to a person of ordinary skill in the art to realize that His control system would also include a program counter to determine the location of a second instruction that includes a pointer to an exception handler. This is because, his control system provides a series of instruction, detection of exception handling conditions and mechanism to invoke an exception handler. Furthermore, it is well know in the art to utilize a program counter to determine the location of the next instruction to be executed.

26. As per claim 27, He teaches (col. 3, lines 32-34) that if an exception condition is detected during the processing operations, to invoke an exception handler in accordance with the processor's precise exception handling model.

Allowable Subject Matter

27. Claims 20 & 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (703)-308-5228. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703)-305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI